PHONONIC

SOLID STATE COOLING WITH PHONONIC:

Optimizing Design and Manufacturing to Meet the Real-World Data Center Demands of TECs

ciena + PHONONIC

- Real-world realistic thermal modeling and design specs, grounded in critical performance, cost and manufacturing trade-offs
- Collaborative design process to enable fully informed trade-offs and decision-making
- Industry-leading performance and design specs, exceeding critical heat flux and power requirements
- Increased manufacturing through-put, co-developed critical binning process

Ciena + Phononic: Collaborative Partnership Improves Performance, Manufacturing Through-Put and Design Flexibility

The explosive growth of AI workloads is placing unprecedented demands on data center networks, driving the need for increasingly advanced optical transceivers and the cooling systems that support them. As transmission distances extend and link speeds escalate, precise temperature stabilization becomes critical to maintaining performance and signal integrity. At the same time, the massive increases in data volume, bandwidth, and latency sensitivity required for AI, machine learning, and inference workloads leave virtually no margin for error. These step-function jumps in performance expectations make it essential to have forward-looking technologies—and design partners—who can collaborate proactively to address emerging challenges and capitalize on new opportunities.

Coherent optical transceivers—like other components—are becoming essential to the architecture of modern AI data centers because they deliver the high-capacity, long-reach connectivity required for on-campus and inter-campus networking. As AI training workloads scale into the multi-petabyte regime and east-west traffic explodes, traditional intensity-modulated direct-detect optics can no longer meet the demands for bandwidth, spectral efficiency, and signal integrity over longer distances. Coherent transceivers use advanced modulation formats and digital signal processing to maintain high performance over multi-kilometer links, enabling seamless expansion of AI fabrics without sacrificing latency or reliability. This allows hyperscalers to build larger, more distributed AI superclusters, support higher-speed interconnects such as 800G and beyond, and ensure stable, deterministic communication between GPUs—ultimately improving training efficiency and reducing job completion times. In such an environment, the pace of innovation has never been greater, and the benefits of collaborative, forward-thinking design have never paid greater dividends.

A Partnership Grounded in a Shared Mission, and Collaborative Design

When Ciena recognized the rapidly evolving dynamics of the optical transceiver market—particularly the trend toward integrating multiple TECs within a single module—the need for a proactive, forward-looking design approach became undeniable. Faced with this complex engineering landscape, Ciena engaged their trusted partners at Phononic to design, and model a groundbreaking thermoelectric and transceiver-package solution that meets both today's demands and tomorrow's opportunities.

The result? A rigorously engineered solution that delivers precise temperature control, improved signal stability, and higher reliability across diverse deployment environments—advancing both the state of transceiver design and Ciena's ability to support the next generation of coherent optical systems.

PHONONIC'S PROPRIETARY APPROACH TO DESIGN:

Collaborative Design, Real-World Realistic Thermal Modeling, Industry-Leading Performance, Efficiency and Cost

OUR PROPRIETARY APPROACH TO DESIGN

At Phononic, we have a proprietary approach to our design process. With 40 million + TECs in the field, this time-tested approach consistently produces the highest quality of results.

Phononic relies on several statistical process control metrics to ensure your application-specific TECs are designed to perfection. We use our state-of-the-art optical imaging techniques combined with Statistical Process Control (SPC) for every TEC manufactured in our assembly factory, as well as ensuring all those TECs' key and critical-to-quality device parameters are in-control.

Phononic also uses Confocal Scanning Acoustic Microscopy (CSAM) to obtain quick, non-destructive analysis of critical device interfaces, such as solder joints. We use this process on 100% of parts to monitor and ensure element/header junction interface integrity.

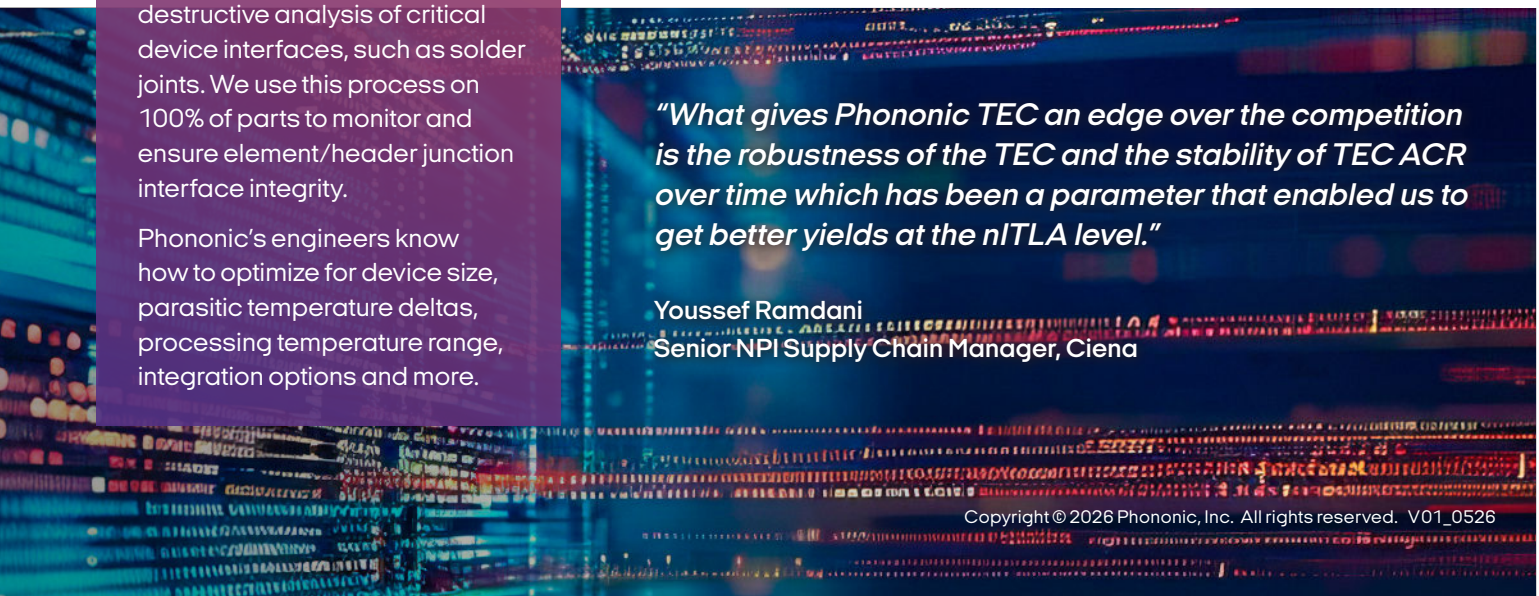
Phononic's engineers know how to optimize for device size, parasitic temperature deltas, processing temperature range, integration options and more.

Deep Design Expertise and Proprietary Real-World Thermal Modeling Illuminates Trade-offs, Guides Decision-Making, and Improves Business Outcomes

As the Ciena team recognized, there are significant mechanical and geometric integration challenges associated with embedding multiple TECs within a constrained transceiver form factor. Each thermoelectric component must be positioned to meet stringent heat-pumping requirements, maintain compliance with the module's volumetric and spatial constraints, and align precisely within the optical and electrical planes to preserve modulation fidelity and optical path stability. To address these complexities, the Ciena team defined three distinct architectural concepts and engaged Phononic to perform detailed design work, conduct multiphysics modeling, and deliver a comparative analysis outlining the thermal performance, mechanical feasibility, and system-level trade-offs associated with each approach.

The Phononic team had a deep understanding of the thermo-mechanical design constraints, manufacturability requirements, and performance targets associated with incorporating multiple TECs into a single transceiver package. With each architectural option, the team engineered an optimized cooling configuration that accounted for device footprint, parasitic thermal resistances, allowable ΔT under load, processing-temperature envelopes, assembly stack-ups, and integration path dependencies.

Through this rigorous design, modeling, and iterative review process, the Ciena team selected a TEC configuration that maximized Qmax, improved COP and electrical efficiency, and integrated seamlessly into the targeted module architecture with minimal impact on assembly complexity or line throughput.



"What gives Phononic TEC an edge over the competition is the robustness of the TEC and the stability of TEC ACR over time which has been a parameter that enabled us to get better yields at the nITLA level."

Youssef Ramdani
Senior NPI Supply Chain Manager, Ciena